I Claim:

1. A memory circuit, comprising:

a memory cell array including a plurality of memory cells, said memory cell array including a plurality of word lines and a plurality of bit lines for addressing said plurality of memory cells;

a plurality of write amplifiers for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines; and

an address decoding circuit for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines.

2. The memory circuit according to claim 1, further comprising:

a plurality of switching devices;

each one of said plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices in order to write the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of said plurality of bit lines addressed by a write address.

3. The memory circuit according to claim 2, wherein said address decoding circuit is configured to simultaneously connect one of said plurality of write amplifiers to assigned ones of said plurality of bit lines depending on the test mode signal.

4. A method for writing data to a memory circuit, which comprises:

providing a memory cell array including a plurality of memory cells;

providing the memory cell array with a plurality of word lines and a plurality of bit lines for addressing the plurality of memory cells;

providing a plurality of write amplifiers for writing to the plurality of memory cells, and assigning each one of the

plurality of write amplifiers to a group of the plurality of bit lines;

simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that the group of the plurality of write amplifiers writes a test datum to a group of the plurality of the memory cells via respectively assigned ones of the plurality of bit lines.

5. The method according to claim 4, which further comprises simultaneously connecting each amplifier in the group of the plurality of write amplifiers to assigned ones of the plurality of the bit lines for writing the test datum.